Claims

1. Isolation interface with a capacitive barrier, comprising

- at the input end of the capacitive barrier an input circuit (A1) with differential outputs for a first and a second logical output signals U1o+ and U1o-, respectively, that are replicas of a transmitted input signal Ui and are complementary to one another,
- a first barrier capacitor (C+) and a second barrier capacitor (C-) for the first and second logical signals U1o+ and U1o-, respectively,
- at the output end of the capacitive barrier, an output circuit (A2) with inputs for a first logical input signal U2i+ and a second logical input signal U2i-, respectively, that are complementary to one another, and the output circuit (A2) comprises a first voltage comparator (Co+) and a second voltage comparator (Co-), and

characterized in

that in the input circuit (A1) a first integrating unit (R1, C1)+ and a second integrating unit (R1, C1)- are provided, across which the first logical output signal U1o+ and the second logical output signal U1o-, respectively, passed and by means of whose time constants the slope rates of the edges of the signals U1o± or the rising and falling-off times of the signals U1o± were adjusted,

and that to an output terminal of the first barrier capacitor (C+) and of the second barrier capacitor (C-) on the one hand and to a common potential terminal of the output circuit (A2) on the other hand, such a first resistor (R+) and a second resistor (R-) are connected

that the time constant of a first differentiating unit (C+, R+) made of the first barrier capacitor (C+) and of the first resistor (R+)

and the time constant of the second differentiating unit (C-, R-) made of the second barrier capacitor (C-) and of the second resistor (R-)

are shorter than the rising and falling-off times of the logical output signals U1o+ and U1o- being the replicas of the transmitted input signal Ui.

2. Isolation interface with a capacitive barrier as recited in claim 1, characterized in

that the first logical input signal U2i+ and the second logical input signal U2i- of the output circuit (A2) are conducted directly to a first and a second inputs, respectively, of the first voltage comparator (Co+) as well as to a second and first inputs, respectively, of the second voltage comparator (Co-)

and that an output of the first voltage comparator (Co+) and an output of the second voltage comparator (Co-) are connected to inputs of a flip-flop (F),

whose output is an output of the isolation interface with the capacitive barrier.

3. Isolation interface with a capacitive barrier as recited in claim 1 or 2, characterized in

that an input of the basic isolation interface (A1, C+, C-, R+, R-, A2) with a capacitive barrier is connected to a control input of a pulse-width modulator (PWM), to whose second input a constant frequency signal is uninterruptedly conducted and whose output is connected to an input of an auxiliary isolation interface provided for transmission over an auxiliary communication channel (ACC),

that the output of the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier and an output of the auxiliary isolation interface for transmission over the auxiliary communication channel (ACC) are connected to inputs of a decision logical circuit (DLC) that provides for a correct logical state of the signal transmitted by the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier,

and that an output of the decision logical circuit (DLC) is the output of the isolation interface with the capacitive barrier.

4. Isolation interface with a capacitive barrier as recited in claim 3, characterized in

that individual output end units of the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier are turned on or off depending upon the state of the modulated signal at the output of the auxiliary isolation interface for the transmission over the auxiliary communication channel (ACC).

5. Method for transmitting a signal through an isolation interface with a capacitive barrier, characterized in

that in an input circuit of the isolation interface with the capacitive barrier by means of an integration with an appropriate time constant the slope rates of the edges or the rising and falling-off times of signal replicas U1o+ and U1o- of the transmitted input signal Ui are adjusted

and that the said signal replicas U1o+ and U1o- are differentiated in a first differentiating unit and in a second differentiating unit, respectively, of the capacitive barrier,

and that the time constants of the first and the second differentiating unit are shorter than the rising and falling-off times of the signal replicas U1o+ and U1o-, respectively, of the transmitted input signal Ui.

6. Method for transmitting a signal through an isolation interface with a capacitive barrier as recited in claim 5, characterized in

that signals U2i± of the derivatives performed in the differentiating units of the capacitive barrier are conducted directly to two voltage comparators comprised in an output circuit of the isolation interface with the capacitive barrier.

7. Method for transmitting a signal through an isolation interface with a capacitive barrier as recited in claim 5 or 6, characterized in

that, besides transmitting the input signal Ui through the basic isolation interface with the capacitive barrier, there is uninterruptedly performed the transmitting of a constant frequency signal Uia, which is pulse-width-modulated with the transmitted input

signal Ui, through an auxiliary isolation interface for transmission over an auxiliary communication channel (ACC)

and that according to a modulation of the transmitted pulse-width-modulated signal Uouta, the logical state of an output signal Uout transmitted by the isolation interface with the capacitive barrier is adjusted.